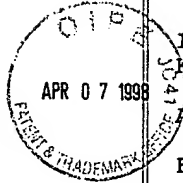


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re Patent Application of :  
Khandros et al. :  
Application No. 08/984,615 : Group Art Unit: 3206  
Filed: December 3, 1997 : Examiner:  
For: SEMICONDUCTOR CHIP PACKAGE : Date: April 2, 1998  
WITH CENTER CONTACTS :  
X

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application. The fee has been calculated as shown below.

CLAIMS AS AMENDED

(1)	(2)	(3)	(4)	(5)	(6)	(7)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PAID FOR	NUMBER OF EXTRA CLAIMS	RATE	ADDL. FEE
TOTAL CLAIMS	* 10	MINUS **	20	= 0	x \$ 22 = \$	0
INDEP. CLAIMS	* 1	MINUS ***	3	= 0	x \$ 82 = \$	0
FEE FOR FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM(S)					\$270 = \$	0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT.....\$						0

- \* If the entry in col. 2 is less than entry in col. 4 write "0" in col. 5.
- \*\* If the "highest number paid for" in this space is less than 20, write "20" in this space.
- \*\*\* If the "highest number paid for" in this space is less than 3, write "3" in this space.

1. ☒ No additional fee is required.
2. ☐ Charge \$ to Deposit Account No. 12-1095. A duplicate copy of this sheet is enclosed.
3. ☐ Please charge any additional fees or credit overpayment to Deposit Account No. 12-1095. A duplicate copy of this sheet is enclosed.

LERNER, DAVID, LITTENBERG,  
KRUMHOLZ & MENTLIK

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J.Wmo

TESSERA 3.3-018 CONT CONT 2.DIV.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Applicant of :  
Khandros et al. : Group Art/Unit: 3206  
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Assistant Commissioner For Patents  
Box Patent Application  
Washington, D.C. 20231

SUPPLEMENTAL PRELIMINARY AMENDMENT

Sir:

Please amend the application as follows:

In the Claims:

Amend claims 61-62, 64-70 as follows:

61. (Amended) A semiconductor chip assembly comprising:

(a) a semiconductor chip having a front surface defining the top of the chip, said front surface including a central region and a peripheral region surrounding said central region, whereby said central region is disposed inwardly of said peripheral region, said chip having central contacts disposed in said central region of said front surface;

(b) a dielectric element overlying said chip front surface, said dielectric element having a first surface facing toward said chip and a second surface

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231 on April 2, 1998.

*Michael J. Doherty*

(Signature)

MICHAEL J. DOHERTY

Typed or Printed Name of Person Signing Certificate